National Centre for Radio Astrophysics
Tata Institute of Fundamental Research
Pune University Campus, Pune -INDIA.

Technical Report on

Design & Implementation of New FE Parameter Control Unit at Antenna Base

Authors:

Navnath Shinde, Sweta Gupta, Ajay Vishwakarma

17 January 2017 _ V1.1

Author : Navnath / Sweta/ Ajay **Verified by :**	**Date of issue:**	**Scope**
Approved by : Ajit Kumar B.	**Status/ Version : Ver.1**	**Internal Technical Report No :**

ACKNOWLEDGEMENT

We are thankful to Prof. Yashwant Gupta (Dean of GMRT) and Prof. S K Ghosh (Center Director of NCRA-TIFR) for giving constant support during this work.

We would also like to express our gratitude towards our group coordinator Shri Ajit Kumar, for his constant guidance and encouragement. We would like to say sincere thanks all our analog lab group members, for time to time sharing and discussing their views for improvement of this new development.

We would also like to thanks analog back-end team for their active participation in mass production, testing and installation of the Developed unit at antenna base.

ABSTRACT

To design and implement a New FE Parameter Control unit with additional Walsh features using CPLD at Antenna Base Receiver. For this purpose, efficient method of 128 bit length Walsh pattern generation logic has been developed.

The logic for Walsh pattern generation forms the main part of the front end control circuit along with various other clock synchronized logics like noise pattern generation, Sequency pattern generation.

The overall architecture for various patterns generation has been programmed in a CPLD using Xilinx Design Tools. The new design is based on CPLD to supersede the existing EPROM based control.

Fig. No.	Name of Figure	Page No.

1. AIM:

As per our aim, we proposed to design and implement a New FE Parameter Control unit with additional Walsh features using CPLD at Antenna Base Receiver.

2. PROBLEM DEFINITION :

The main aim of the design is to make Front End control unit to control FE parameters through a dedicated MCM in the ABR. This involves improving the Walsh card PCB in the D-49 PIU. This PCB consists of digital circuitry having a number of IC's with differential line driver circuitry for long distance transmission of signals from the antenna base to the front end. All this Digital circuitry part can be simulated in the CPLD and thus saving the cost and providing better performance in comparison to the EPROM based circuitry of the existing Walsh card. Hence, the new Walsh card consists of the CPLD and differential line driver circuitry with minimum Components and thus size. Besides reducing the size, additional functionality and features has been added to the card by programming the CPLD in order to improve the overall performance and provide more flexibility to the user for better analysis while observation.

3. Existing Front End Control through MCM-2:

The Monitor and Control Module-2 (MCM-2) in the D-49 control PIU of LO Synthesizer at ABR, controls the selection of various patterns which will be combined with the RF signals at the front-end and the control of front end MCM(MCM-5), as per the online commands issued by the user in the control room. A Walsh card PCB WNG_RO in the PIU is used for this purpose and consists of EPROM which is encoded with the various patterns. This PCB also generates the various monitoring signals for enabling the Monitoring card PCB in the D-49 PIU. An interface panel with a 10-way terminal strip has been provided at the rear of the ABR rack to bring the patterns from rear of D-49 PIU to a convenient location for connecting to the 10-core front-end cable.

Pattern requirements for the Front End System from the LO Synthesizer:

- Generation and selection of noise patterns for noise switching.
- Generation and selection of Walsh patterns for Walsh switching at the front end.
- Switching ON and OFF the front end MCM.

3.1 Selection of WALSH and NOISE Patterns in Existing Design:

The 128 Walsh patterns have been divided into two groups as *High Group* and *Low Group*. The control signals required for enabling/disabling Walsh Patterns, selection of *High Group* or *Low Group* and Noise ON/OFF are generated in the control PIU D-49 in the ABR at the base of each antenna . The Digital Plug-In-Unit (PIU), D-49 of the Local Oscillator (LO) Synthesizer in the ABR is the control PIU and contains the following PCBs:

- The MCM PCB, which is the interface to the LO systems.
- The Reset PCB RESET_R1.
- The Control PCB CON_R2.
- The Walsh and Noise Generator control PCB WNG_RO with ID Code D 85, used in the Monitoring scheme of the synthesizer as well as controlling a few parameters of the front-end at the antenna.
- The Power supply PCB.
- The Monitor multiplexer PCB, MON32_R0.
- The front panel LED indicator PCB, LED49_R0.

A Block Diagram of the control PIU-D49 is shown in the following figure:

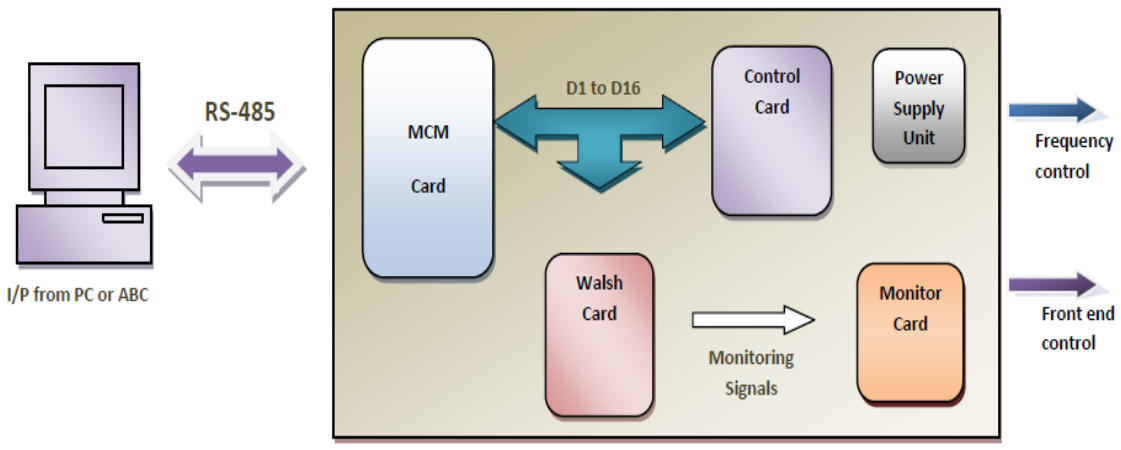
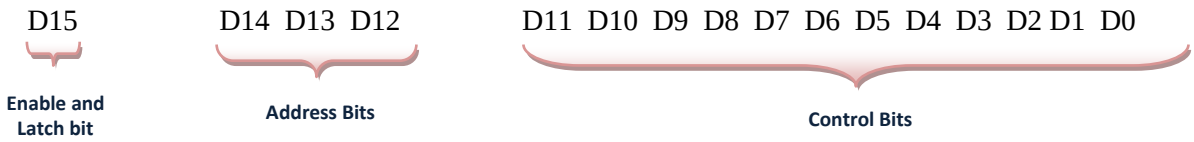


Figure 1: Block Diagram of existing D-49 PIU

MCMs are general purpose microcontroller based cards which provide 16 TTL digital control outputs and can monitor up to 64 input analog signals. These MCMs are the interface to all the settable GMRT subsystems, like the front-ends, the LOs, the

attenuators, etc. In detail, at each antenna, MCM 5 is the interface to the front end system, while MCMs 2, 3, and 10 are the interface to the LO and IF systems. Input to MCM card is provided from PC or ABC through a RS-485 line. These inputs are the various commands issued by a user for setting the parameters of the electronics and for monitoring a range of parameters. The 16 bit digital data from MCM card is divided into three parts as under:



The address bits for address are used to obtain, in principle a total of 8×12=96 independent control bits. Also, the Enable and Latch bit helps in latching the data so that any Address Group can be set without worrying about the control bits already set through another address group.

- Address groups 0, 1, 2 and 4 are used for the control of GMRT synthesizer to set the required frequency. The controls under these groups are controlled using the Control card PCB.
- Address group 6 contains control bits used for monitoring. These controls are operated by the Walsh card PCB.
- Address group 7 contains control bits used for setting a few of the front-end parameters related to Walsh switching. The controls under this group are controlled by the Walsh card PCB.
- Address groups 3 and 5 are not used.

The digital data from MCM is available on 20 pin FRC Connector and then sent to control card PCB CON_R2 and Walsh and noise generation PCB WNG_RO. Depending on the address group selected (as stated above), Control card PCB or the Walsh card PCB comes into operation and gives the required outputs as per the control bits selected. Thus WNG_RO PCB comes into operation by group 6 and group 7 selections and is used for generating monitoring outputs and selection of noise ON/OFF or Walsh enable/disable respectively.

The block diagram of the existing Walsh Card WNG_RO is as follows:

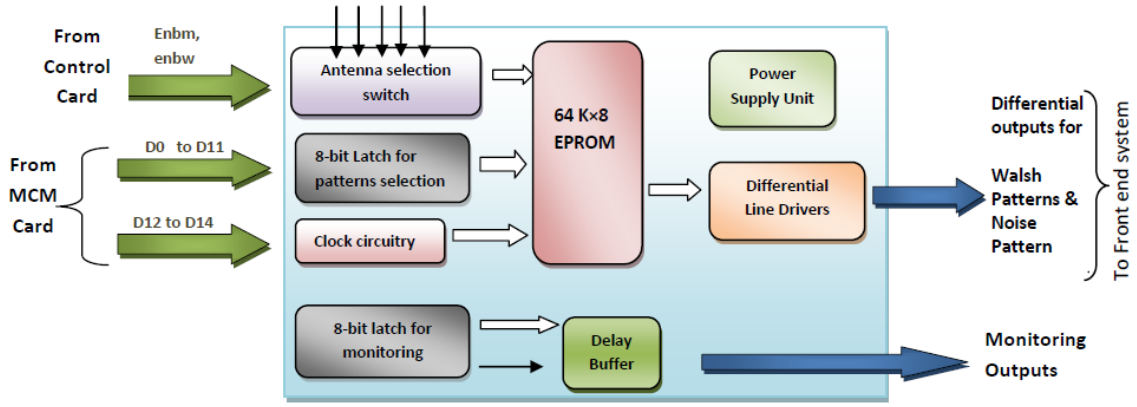


Figure 2: Block Diagram of EPROM based Walsh Card

4. Introduction of new CPLD based FE Control Unit:

The heart of the new Walsh and FE control card unit is a CPLD which contains the main logic for various pattern generations and control for MCM-5 instead of EPROM. In case of the new Walsh and FE control card, we are generating a desired pattern based on the selection inputs at that particular instant, instead of storing them in advance.

The new Walsh card can be used for generating only **Cal patterns** or the Sal patterns, (the 128 bit length) in comparison to the existing circuit which uses both the Cal and the Sal patterns, along with NG pattern and Sequency which are burned in EEPROM.

Additional functionality can easily be added by reprogramming the CPLD at any time in future to provide more flexibility to the users.

The CPLD based circuit controls the functions under the Group-7 (FE control and Walsh). Thus the CPLD has been programmed with logic for these operations and placed in the Walsh card circuit along with few other components.

4.1 Features and Advantages:

❖ ***Consist of a programmable Walsh pattern generator:***

Instead of storing all the 128 Walsh patterns, Sequency pattern and noise pattern in advance, we now generate the desired pattern dynamically as per the requirements.

❖ *Independent channel selection facility for taking the Walsh patterns output :*

The user can now have the provision to select independent channels of a particular antenna and add Walsh patterns on these channels as follows:

- ✓ To add Walsh pattern on one of the channels, i.e., Channel (CH1) 1 or Channel 2 (CH2) while disabling Walsh pattern on the other.
- ✓ To add different Walsh patterns on both the channels from Group-1 or Group-2. For CH-1 or CH-2, respectively, at the same time.
- ✓ To add the CH-1 Walsh pattern on CH-2.
- ✓ To add the CH-2 Walsh pattern on CH-2.
- ✓ Independent Basic Walsh pattern on both channels

❖ *Variable time period selection for all the patterns :*

The complete 128 bits pattern for Walsh function, Sequency and the pattern for noise may be needed for certain time duration depending on the need of the user and the system. The new circuit thus gives the facility to select variable time period for each of the bits of these patterns. The user can select either a **4ms, 8ms, 16ms or 32ms** duration time period each bit of every pattern.

❖ *Independent time period of noise patterns and Walsh patterns :*

The length and time period of noise patterns and 128-bits Walsh patterns, Sequency patterns is independent of each other, i.e., the time period of noise pattern can be varied while keeping the time period for Walsh pattern and Sequency pattern constant and vice-versa.

❖ *Only CAL patterns selection :*

In order to remove the phase ambiguity between Cal and Sal patterns, only Cal patterns have been used for the antennae.

4.2 Block Diagram of FE and Walsh Control Card:

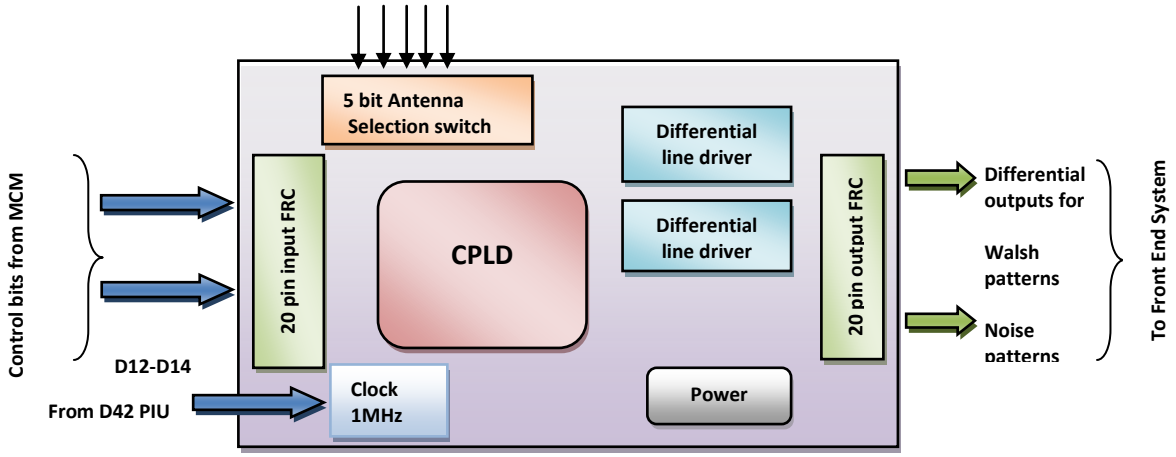


Figure 3- Block diagram of new Walsh card

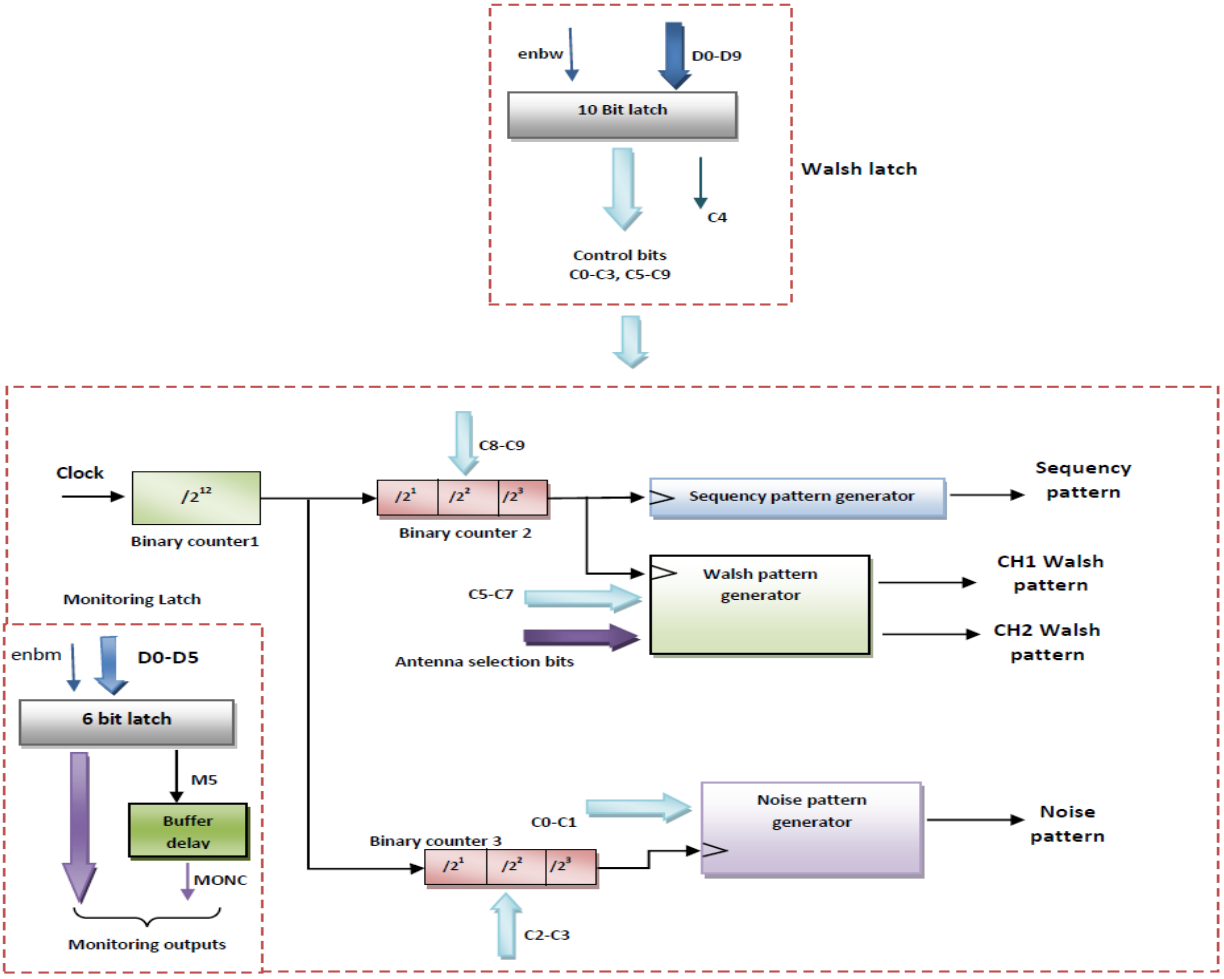


Figure 4: Diagram for structure view of Blocks and its logic for implemented in CPLD

Table 1.1- Truth Table for Clock Circuitry

Frequency selection bits for Noise pattern generator		Frequency selection bits for Walsh pattern generator		Selected Clock frequency ($F_{in}/2^n$)	Time period
D3	**D2**	**D9**	**D8**	**n**	**($1/F_{in}$)**
0	*0*	0	0	0	**4 ms**
0	1	0	1	1	**8 ms**
1	0	1	0	2	**16 ms**
1	1	1	1	3	**32 ms**

***F_{in}=1.0 MHz**

Table 1.2- Truth Table for Noise Pattern selection

Pattern selection bits		Noise pattern	Duty Cycle
Bit D1=0	***Bit D0**=0*	NGN1	**0% (Noise OFF)**
0	1	NGN2	**25%**
1	0	NGN3	**50%**
1	1	NGN4	**100%**

Table 1.3-Truth Table for Walsh Generator

Antenna selection Bits					Channel selection bits			Channel	
DS0	DS1	DS2	DS3	DS4	D7	D6	D5	CH1	CH2
X	X	X	X	x	0	0	0	WALSH OFF	WALSH OFF
0	0	0	0	0	0	0	1	CAL 1	WALSH OFF
					0	1	0	WALSH OFF	CAL 32
					0	1	1	CAL 1	CAL 32
					1	0	0	CAL1	CAL1
					1	0	1	CAL32	CAL32
					1	1	0	BASIC WALSH	WALSH OFF
					1	1	1	WALSH OFF	BASIC WALSH
0	0	0	0	1	0	0	1	CAL 2	WALSH OFF
					0	1	0	WALSH OFF	CAL 33
					0	1	1	CAL 2	CAL 33
					1	0	0	CAL2	CAL2
					1	0	1	CAL33	CAL33
					1	1	0	BASIC WALSH	WALSH OFF
					1	1	1	WALSH OFF	BASIC WALSH
0	0	0	1	0	0	0	1	CAL 3	WALSH OFF
					0	1	0	WALSH OFF	CAL 34
					0	1	1	CAL 3	CAL 3
					1	0	0	CAL3	CAL3
					1	0	1	CAL34	CAL34
					1	1	0	BASIC WALSH	WALSH OFF
					1	1	1	WALSH OFF	BASIC WALSH

……and sequence to be continued.

Note: Pls refer the Annexure-1 for details of command file and referral commands

4.3 Schematic for CPLD based FE control card:

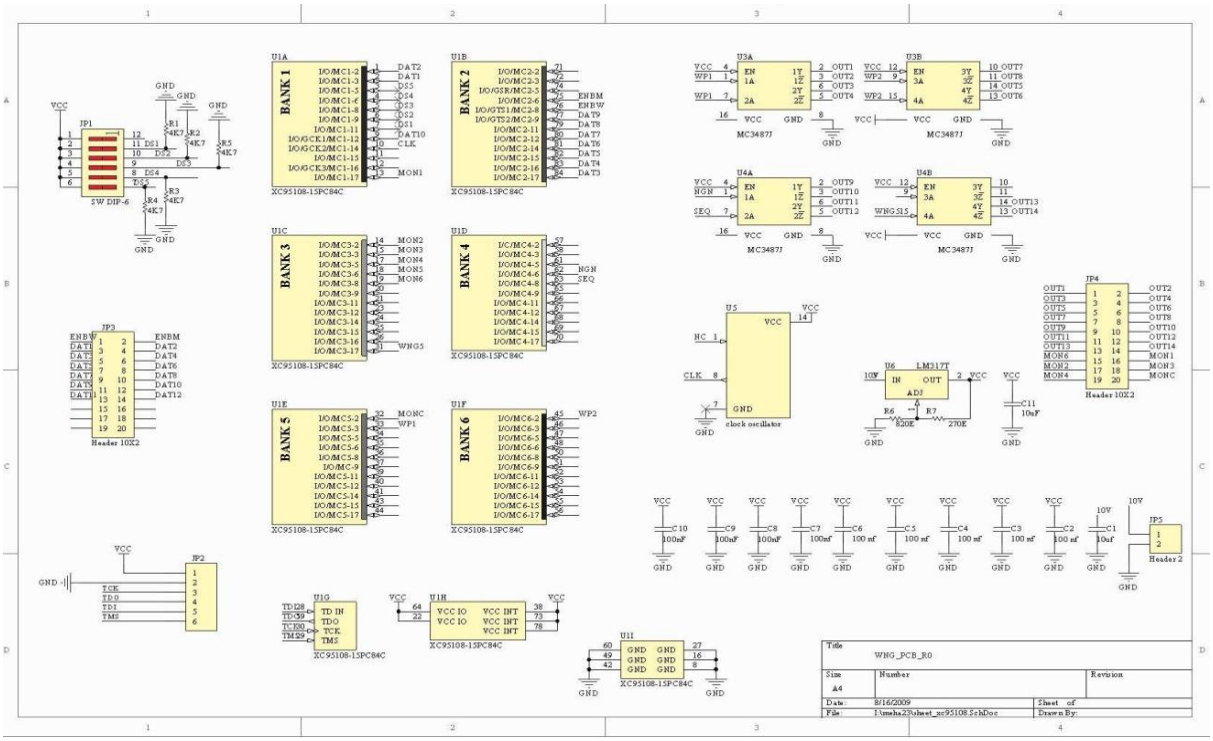


Figure 5: Schematic Diagram for CPLD based FE control card

5. Requirement of dedicated MCM unit:

This idea will add-on a dedicated new MCM unit (named as MCM4). The main limitation of CPLD is the resources availability to accommodate the program logic. Various program constraints are opted to optimize the new developed program to fit in the CPLD XC95108, resources proceeding to 85%. The remaining resources must be available for future addition and expansion as per the requirement of the users.

In this view, a dedicated CPLD card with MCM unit has been designed and integrated in unit to control the required FES parameters. This will facilitate the system as independent control of FES parameters and reduce the failure due to combined systems, thus to improve the MTBF of the system

5.1 Features of dedicated MCM4 UNIT:

1. This will work as a specific UNIT for FE parameter control.
2. All present functionalities will be supported as previous EPROM based FE control card.
3. Additional Walsh pattern control functionalities have been added.
4. The Clock for system design is synced with a 1MHz clock signal (D42- 1 MHz generation PIU of LOR system) which is locked to GMRT Frequency and Time reference at each antenna.

5.2 PIU Integration:

This newly designed PIU named as MCM-4 contains the following PCBs:

- The MCM PCB.
- The Walsh and Noise Generator CPLD based PCB
- The Power supply PCB.
- The front panel LED indicator PCB.

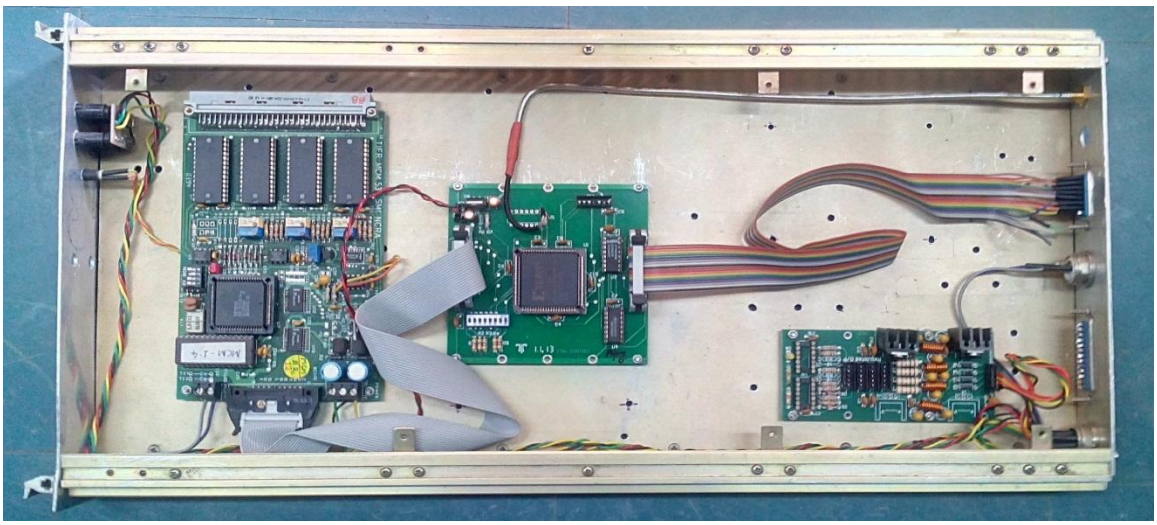


Figure 6: Snapshot of MCM-4 CPLD based FE and Walsh PIU

6. Prototype System Lab Test Setup:

The integrated unit has been tested in lab for all FE control commands which are listed in Annexure1. Also detailed test report for testing all commands has been prepared which will be useful for detailed measurement of each commands for individual PIU.

Following are the snapshot of the Lab Test Setup and Test report:

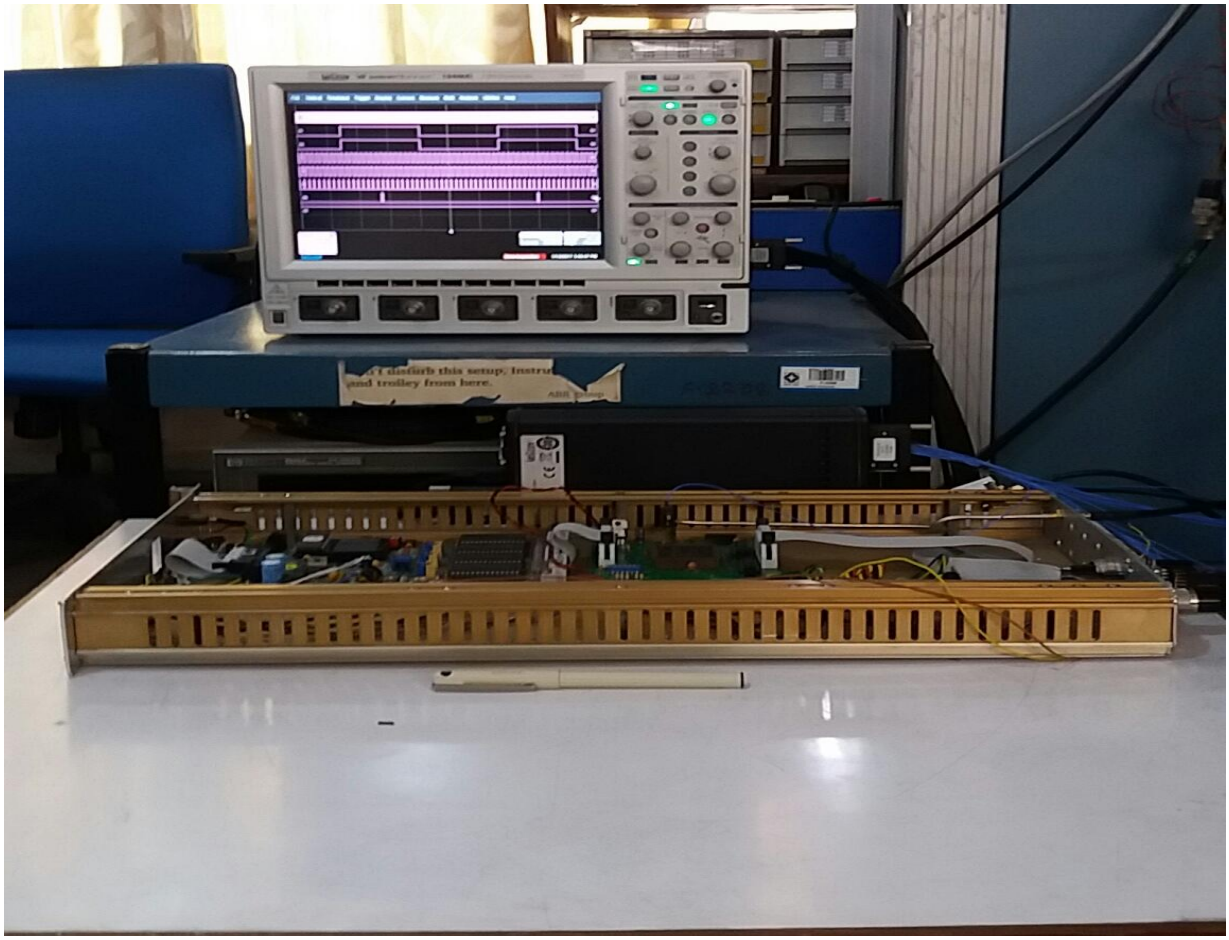


Figure 7: Snapshot of CPLD based FE and Walsh PIU lab test setup

Test report of Walsh PIU No. …… Date…… Sign……

Command File name, Hex codes	Online commands	Patterns to check	Lab. Test	Ant. Test
FE ON **70 10 f0 00**	MCM selection **1**	High		
FE OFF **70 00 f0 00**	MCM selection **0**	Low		
NG ON **70 03 f0 03**	NG time domain **100**	High		
NG 25 **70 01 f0 01**	NG time domain **25**	4 + 12 mSec		
NG 50 **70 02 f0 02**	NG time domain **50**	8 + 8 mSec		
NG OFF **70 00 f0 00**	NG time domain **0**	Low		
NG 50 –F1 **70 06 f0 06**	NG Freq. Selc. /2 (50) **1**	16 + 16 mSec		
NG 50 –F2 **70 0a f0 0a**	NG Freq. Selc./4 (50) **2**	32 + 32 mSec		
NG 50 –F3 **70 0e f0 0e**	NG Freq. Selc./8 (50) **3**	64 + 64 mSec		
WL1 **70 20 f0 20**	Walsh Pattern Gen. **1**	262 + 262 mSec		
WL2 **70 40 f0 40**	Walsh Pattern Gen. **2**	8 + 8 mSec		
WLB **70 60 f0 60**	Walsh Pattern Gen. **3**	262 + 262 mSec, 8 + 8 mSec		
WL1 (1 &2) **70 80 f0 80**	Walsh Pattern Gen. **4**	262 + 262 mSec, 262 + 262 mSec		
WL2 (1&2) **70 a0 f0 a0**	Walsh Pattern Gen. **5**	8 + 8 mSec, 8 + 8 mSec		
	Walsh Pattern Gen. **6**	262 + 262 mSec, **CH-2 OFF**		
	Walsh Pattern Gen. **7**	262 + 262 mSec, **CH-1 OFF**		
	Walsh Pattern Gen. **0**	Low (WL1 & WL2)		
	Walsh Freq. Selection (3) **0**	262 + 262 mSec, 8 + 8 mSec		
WLB- F1 % 2 **71 60 f1 60**	Walsh Freq. Selection **1**	524 + 524 mSec, 16 + 16 mSec		
WLB- F2 % 4 **72 60 f2 60**	Walsh Freq. Selection **2**	1048 + 1048 mSec, 32 + 32 mSec		
WLB- F3 % 8 **73 60 f3 60**	Walsh Freq. Selection **3**	2096 + 2096 mSec, 64 + 64 mSec		

Figure 8: Snapshot of CPLD based FE and Walsh PIU Test Report

Following is the plot for MALL Command Output which Enable 25% duty cycle noise pattern, different Walsh patterns on both channels of the selected antenna:

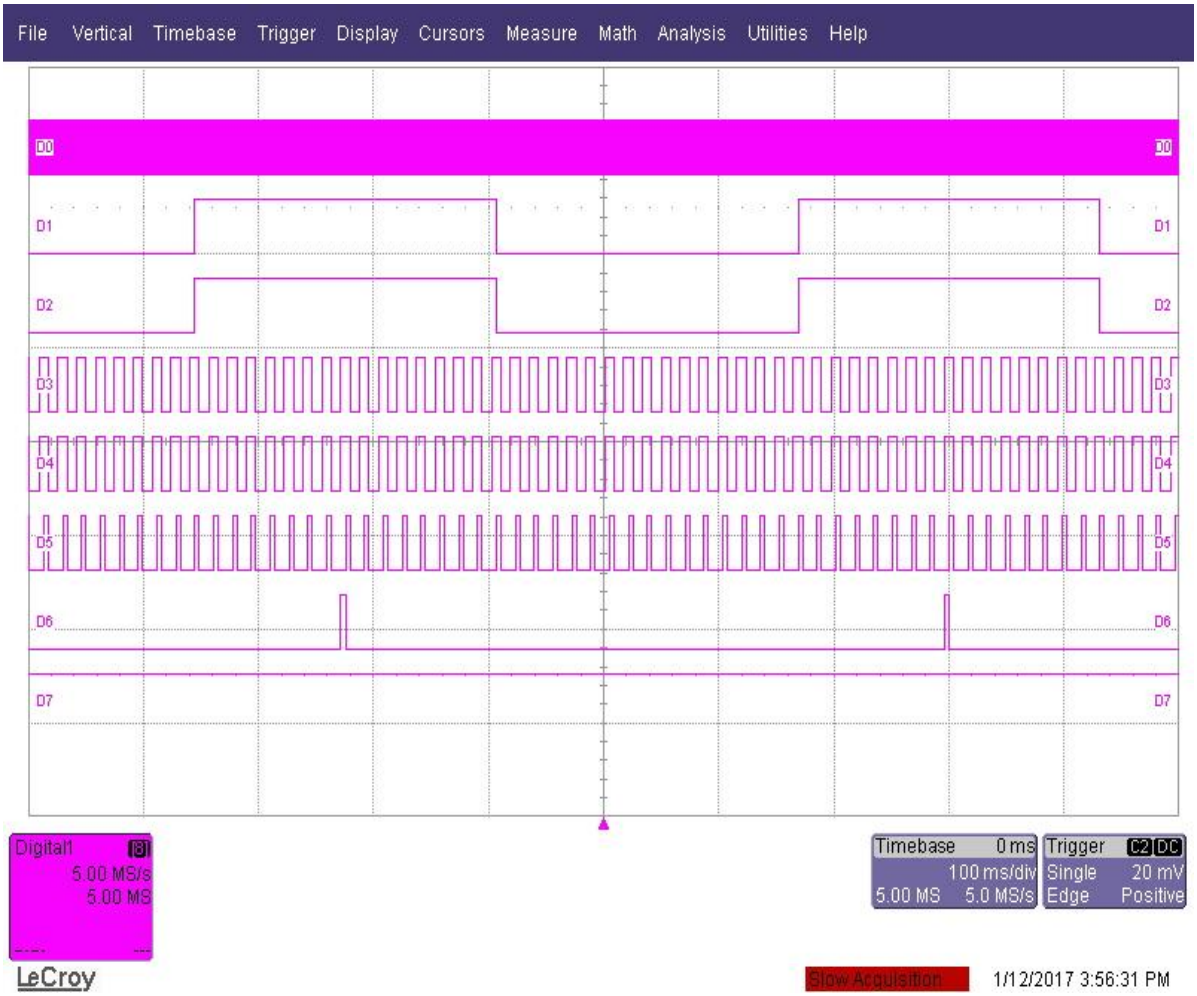


Figure 9: Snapshot of MALL Command Output Waveform

7. Prototype installation and testing at ABR:

For prototype installation at antenna base, command lines were needed to be modified for the newly added Walsh and Noise features.
With help from operation group, “cdsetm4” command set has created which consists of all the required commands.
The SOP for issuing the Control command for FES parameters as follows:

Step 1: Add MCM-4 in 'online'

Step 2: Use 'cdsetm4' for FES parameter setting

Step 3: 'run fe4mcm’ to execute parameters setting

Presently this system has successfully installed and functional at C02 and C05 Antenna since November22, 2016. All the existing FE control and Walsh commands are supported by this newly developed FE Parameter Control unit.

Following is the snapshot of the system at ABR :

Figure 10: Snapshot of FE & Walsh Control PIU at C10 Antenna

Command List in "cdsetm4" for the new parameters:

* FRONT END PARAMETERS. Give 1419 only for full 1420 band selection.
* select freq. of observation
(50/150/235/290,350,410,470,325/600,685,725,770,850/1060,1170,1280,1390,1420 MHz.)
1390

* select solar attenuator (0/14/30/44 dB. -1 for FE Termination.)
0

* select polarisation unswapped(0) or swapped(1)
0

* select cal-noise level.(E-HI(0)/HI(1)/MED(2)/LO(3) (-1 for RF OFF).)
0

* LO PARAMETERS. * select LO freq.(100 - 1600 MHz)
540
540

* IF PARAMETERS. (Default is 14 14)
* select pre_attenuator & post_attenuator for CH1.(0,2,4,...,30 dB)
4
10

* select pre_attenuator & post_attenuator for CH2.(0,2,4,...,30 dB)
4
10

* select IF band width for CH1 & CH2 resp.(6/16/32 MHz).
32
32

* select ALC OFF(0) or ON(1). for CH1 and CH2
1
1

*** New parameters being added :**

* enter NG in time domain (0,25,50 or 100) percent duty-cycle
* CH1 , CH2
0

* enter NG Frequency Selection for CH1, CH2 (0- Fin/1, 1- Fin/2, 2- Fin/4, 3- Fin/8)
0

* MCM Selection 0 - OFF 1 - ON
* CH1, CH2
0

* enter Walsh Pattern Generation
* [0 - WalshOff, 1 - CH1:Cal1 CH2:WalshOff, 2 - CH1:WalshOff CH2:Cal32]
* [3 - CH1:Cal1 CH2:Cal32, 4 - Cal1, 5 - Cal32]
* [6 - CH1:Basic , CH2:WalshOff, 7 - CH1:WalshOff CH2:Basic]
0

* Walsh Frequency Selection for CH1, CH2 (0- Fin/1, 1- Fin/2, 2- Fin/4, 3- Fin/8)
0

8. Further Development Scope:

This logic is presently implemented in Xilinx XC95108PC15 CPLD. To add more counters for further extending the time periods, this could be finalized by the Users depending upon their requirements. It will increase hardware resources requirement of the CPLD but this can be overcome by using a CPLD of higher macro cells such as XC95144, or higher from XC9500 family of Xilinx CPLDs, etc.

9. Bill of Material for MCM4 PIU:

SR No.	Units	Quantity
1	CPLD Card	1
2	MCM Card	1

		BILL OF MATERIALS FOR CPLD Card					
SR No.	Description	Type / Make		Designator	Value		Quantity
1	Capacitor	Ceramic		C2, C3, C4, C5, C6, C7, C8, C9, C10	100kpF		9
		Electrolytic		C1, C11	10uF/50 V		2
2	IC base	PLCC		U1	84 pin		1
3	IC base	DIP		U3, U4	16 pin		2
4	IC 'XC95108	Xilinx (CPLD) PC84		U1	84 pin		1
5	IC 3487	Line Driver		U3, U4	3487		2
6	IC LM317	Volt. Regulator		U6	LM317		1
7	FRC male	FRC		JP3, JP4	20 pin		2
8	DIP Switch	DIP		JP1	6 pin		1
9	Relimate Connector	Male		JP5	3 pin		1
		Male		JP2	6 pin		1
10	Resistor	CFR		R1, R2, R3, R4, R5	4K7		5
		CFR		R6	820E		1
		CFR		R7	270E		1

Table 1.4: Bill of Material for Walsh PIU

Annexure-1

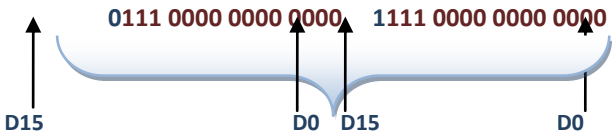
Command file:

Command files contain the 32 bit HEX words given to MCM through the computer. Each 16 bit word in the 32 bits word indicates what function is to be performed by the circuit. In a command file, 32 bit data is to be entered, where, the first 16 bits are for low on D15 enable bit and the next 16 bits are for a high on the enable bit D15. This gives a low to high transition on the enable bit D15 so that the decoder in the control card will generate a corresponding low or high on the group-6 or group-7 enable bit leading to a transition on this bit. This in turn will enable the latches which are positive edge triggered.

For example, the following 32 bit HEX command format is to be followed as shown below. This command simply selects the group-7 by enabling enbw. The 32 bit binary code is given next.

HEX CODE:
7000 F000

BINARY CODE:



32- Bits binary code

A list of command files that were used for testing has been given below with their names, the corresponding HEX codes with the ON bits in the first 12 control bits of the 16 bits sequence, and the desired function:

Command file name	Function	Hex codes	ON bits
FEON	Switch on the front end MCM	7010 F010	D4 is high
FEOF	Switch OFF front end MCM	7000 F000	All b12 bits are low
NGON	Enable 100% duty cycle noise pattern	7003 F003	D0, D1 are high
NG50	Enable 50% duty cycle noise pattern	7002 F002	D1 is high
NG25	Enable 25% duty cycle noise pattern	7001 F000	D0 is high
NGOF	Noise off	7000 F000	All 15 bits are off
WL1	Enable Walsh pattern only on channel 1 of the selected antenna	7020 F020	D5 is high
WL2	Enable Walsh pattern only on channel 2 of the selected antenna	7040 F040	D6 is high
WLB	Enable Walsh patterns on both the channels of the selected antenna	7060 F060	D5, D6 are high
WL1-CH12	Enable channel 1 Walsh pattern on both channels of selected antenna	7080 F080	D7 is high
WL2-CH12	Enable channel 2 Walsh pattern on both the channels of the selected antenna	70A0 F0A0	D5, D7 are high
NG50-F1	Enable divide by 2 frequency selection for 50% duty cycle noise pattern	7006 F006	D1, D2 are high
NG50-F2	Enable divide by 4 frequency selection for 50% duty cycle noise pattern	700A F00A	D1, D3 are high
NG50-F3	Enable divide by 8 frequency selection for 50% duty cycle noise pattern	700E F00E	D1, D2, D3 are high
WLB-F1	Enable divide by 2 frequency selection for different Walsh patterns on both the channels of the selected antenna	7160 F160	D5, D6, D8 are high
WLB-F2	Enable divide by 4 frequency selection for different Walsh patterns on both the channels of the selected antenna	7260 F260	D5, D6, D8 are high
WLB-F3	Enable divide by 8 frequency selection for different Walsh patterns on both the channels of the selected antenna	7360 F360	D5, D6, D8, D9 are high
MALL	Enable 25% duty cycle noise pattern, different Walsh patterns on both channels of the selected antenna	7071 F071	D0, D4, D5, D6 are high
MON	Enable the monitoring controls	603F E03F	D0, D1, D2, D3, D4 are high
BASIC WL1-CH1	Enable 50% duty cycle Walsh patterns on channels 1	70C0 F0C0	
BASIC WL1-CH2	Enable 50% duty cycle Walsh patterns on channels 2	70E0 F0E0	

Table 1.5: Referral List of command files used for testing the circuit